# 8x931AA, 8x931HA
# USB Peripheral Controller

## Specification Update

***August 1998***

**Notice:** The 8*x*931AA/HA may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number: 273140-006

# Contents

# Revision History

| Date | Version | Description |
|---|---|---|
| 10/22/97 | 001 | This is a new Specification Update document. The initial stepping (A-0) of the 8x931AA/HA USB peripheral controller is for prototype purposes only and will not be used as production material. |
| 2/9/98 | 002 | Added B-0 stepping of the 8*x*931AA/HA.<br>Added Specification Change number 2.<br>Added Specification Clarification number 1.<br>Added Documentation Change number 3. |
| 3/17/98 | 003 | Added Specification Change number 3. |
| 6/1/98 | 004 | Added Erratum number 5.<br>Added Specification Change number 4. |
| 7/6/98 | 005 | Added Specification Clarification number 2.<br>Added Documentation Change numbers 4 and 5. |
| 8/5/98 | 006 | Added B-1 stepping of the 8x931AA/HA. |

# Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents/Related Documents

| Title | Order Number |
|---|---|
| 8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual | 273102 |
| 8x931AA, 8x931HA Universal Serial Bus Peripheral Controller Data Sheet | 273108 |

## Nomenclature

**Errata** are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

***Note:*** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

# Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8x931AA/HA products. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

| | |
|---|---|
| X: | Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping. |
| (No mark) | |
| or (Blank box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### Page

| | |
|---|---|
| (Page): | Page location of item in this document. |

### Status

| | |
|---|---|
| Doc: | Document change or update will be implemented. |
| Fix: | This erratum is intended to be fixed in a future step of the component. |
| Fixed: | This erratum has been previously fixed. |
| NoFix: | There are no plans to fix this erratum. |
| Eval: | Plans to fix this erratum are under evaluation. |

### Row

| | |
|---|---|
| | Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document. |

# Errata

| No. | Steppings | | | Page | Status | ERRATA |
|---|---|---|---|---|---|---|
| | A-0 | B-0 | B-1 | | | |
| 1 | X | | | 11 | Fixed | USB VCRS Electrical Characteristics Marginality |
| 2 | X | | | 11 | Fixed | Full-speed Receive FIFO Overflow |
| 3 | X | | | 11 | Fixed | Excessive LED Current |
| 4 | X | | | 12 | Fixed | Isochronous Transfer RXCNT Errata |
| 5 | X | X | | 13 | Fixed | 8x931Ax, 8x931Hx Cold-Boot Errata |

# Specification Changes

| No. | Steppings | | | Page | Status | SPECIFICATION CHANGES |
|---|---|---|---|---|---|---|
| | A-0 | B-0 | B-1 | | | |
| 1 | X | X | | 15 | Doc | The initial 8x931AA and 8x931HA devices will only be available in 68-pin PLCC packages |
| 2 | X | X | X | 15 | Doc | ECAP usage to supply 3.0-3.1 volts for 1.5K pullup. |
| 3 | X | X | X | 15 | Doc | Reduced Float Waveform Iol/IoH Load Value to +/- 1mA. |
| 4 | X | X | X | 15 | Doc | Series Resistor Requirement for Impedance Matching Changed to 22 Ohms (no longer 27 – 33 ohms) |

# Specification Clarifications

| No. | Steppings | | | Page | Status | SPECIFICATION CLARIFICATIONS |
|---|---|---|---|---|---|---|
| | A-0 | B-0 | B-1 | | | |
| 1 | X | X | X | 16 | Doc | P3.6 and P3.7 Low Going Spike |
| 2 | X | X | X | 16 | Doc | PCON GF0 and GF1 Flags are Not Cleared on USB Reset |

# Documentation Changes

| No. | Document Revision | Page | Status | DOCUMENTATION CHANGES |
|---|---|---|---|---|
| 1 | 001 | 17 | Doc | Change Name of Supply Voltage Pins from “Vccp” to “Vcc”. |
| 2 | 001 | 17 | Doc | Change Name of Circuit Ground Pins from “Vssp” to “Vss”. |
| 3 | 002 | 17 | Doc | Product Nomenclature |
| 4 | 005 | 17 | Doc | QFP Package Information Added |
| 5 | 005 | 22 | Doc | Reset Circuitry Referred to in the Cold Boot Errata Added |

# *Identification Information*

## Markings

| Product | Part Number | Stepping | Marking | Package | Comment |
|---|---|---|---|---|---|
| 8x931AA | N83931Ax | A-0 | Q8454 | 68ld PLCC | The initial stepping (A-0) of the 8x931AA/HA USB peripheral controller is for prototype purposes only and will not be used as production material. |
| | N80931AA0 | | Q885 | | |
| 8x931HA | N83931Hx | A-0 | Q8453 | 68ld PLCC | |
| | N80931HA0 | | Q887 | | |
| 8x931AA | N80931AA1 | B-0 | Q891 | 68ld PLCC | This is the second stepping (B-0) of the 8x931AA/HA USB peripheral controller. |
| 8x931HA | N80931HA1 | | Q893 | | |
| 8x931AA | N80931AA2 | B-1 | Q981 | 68ld PLCC | This is the third stepping (B-1) of the 8x931AA/HA USB peripheral controller. |
| 8x931HA | N80931HA2 | | Q980 | | |
| 8x931AA | S80931AA2 | | Q987 | 64ld MQFP | |
| 8x931HA | S80931HA2 | | Q985 | | |

# Errata

## 1. USB VCRS Electrical Characteristics Marginality

**Problem:** The device shows marginality on passing the output signal crossover voltage (VCRS) electrical characteristics (refer to section 7.3.2, Bus Timing/Electrical Characteristics, of the Universal Serial Bus Specification, Rev. 1.0).

**Implication:** This problem occasionally causes the host PC to fail to recognize signals sent by the device, resulting in the termination of communication with the device. Devices connected downstream from an 8x931HA hub may also fail to recognize downstream signaling from the hub and result in failure or incorrect operation of those devices. Downstream port 3 is more susceptible to this failure.

**Workaround:** There is no workaround, although screening samples may eliminate devices that exhibit this marginality.

**Status:** Fixed. Refer to “Summary Table of Changes” to determine the affected stepping(s).

## 2. Full-speed Receive FIFO Overflow

**Problem:** When the host PC sends 1 byte more than the FIFO can receive, the device may respond with an ACK. The problem typically occurs when the following conditions are met:

- Must be operating as a full-speed device (12Mbps). The failure does not occur in low-speed mode (1.5Mbps).
- Occurs with low clock mode enabled (LC, PCON.5 = 1).
- Host sends 9 bytes to an 8 byte FIFO (endpoint 0 and 2) or 17 bytes to a 16 byte FIFO (endpoint 1).
- The RXFLG, RXSTAT and RXCNTL registers contain incorrect values since the data was acknowledged instead of a timeout condition occurring. The RXOVF bit (overflow flag) is set, but the RXFIF, RXFULL, RXSEQ, and RXACK bits are also set.

**Implication:** During normal operation, the host PC should never send more bytes than an endpoint can handle. If this occurs, it could be a sign of a host problem. Data sent from the host PC to the device becomes corrupted, as bytes are lost due to the data packet being larger than what the receiving FIFO can store.

**Workaround:** To prevent a potential problem, low clock mode must be disabled in hub or full-speed hubless devices. Low-speed devices are not affected. Firmware workaround is possible. This requires firmware overhead to check for FIFO status, in addition to transaction status, to clear the error condition.

**Status:** Fixed. Refer to “Summary Table of Changes” to determine the affected stepping(s).

## 3. Excessive LED Current

**Problem:** Pins LED3:0 were designed to drive LEDs connected directly to Vcc. The LED driver is too strong, causing the chip to sink excessive current.

**Implication:** When all the LED drivers are turned on at the same time, the current sinking capability of the device will be exceeded, causing excessive heating and reducing reliability of the device.

**Workaround:** Using a 250 ohm resistor in series with each LED, limit the sink current of the device. This will avoid excessive heating and increase device reliability.

**Status:** Fixed. Refer to “Summary Table of Changes” to determine the affected stepping(s).

## 4. Isochronous Transfer RXCNT Errata

**Problem:** When the 8x931 is configured to use dual packet mode in isochronous transfer, the receive FIFO count register (RXCNTx) of the new data packet is corrupted if the *read completion* of the previous data packet (Setting RXFFRC bit) coincides with *receive done* of the new data packet.

**Implication:** When this problem occurs, the 8x931 will read an incorrect value from the RXCNTx register on the new data packet and hence read an incorrect number of bytes from the receive FIFO. When this occurs, the data read will be either shorter or longer than that actually received, the data read will be incorrect, and the receive FIFO will overflow or underrun.

**Workaround:** At the end of an isochronous data read in the start of frame (SOF) ISR, do **not** release the RXFIFO by setting the RXFFRC bit. In the very beginning of the next SOF interrupt service routine, before the next OUT token arrives, set the RXFFRC bit to release the RXFIFO that was read in the previous frame. This will prevent the *read completion* of the previous data packet (setting RXFFRC bit) from coinciding with the *receive done* of the new data packet. A firmware example of a workaround is shown in Figure 1.

**Status:** Fixed. Refer to “Summary Table of Changes” to determine the affected stepping(s).

**Figure 1. Isochronous Transfer RXCNTx Errata Firmware Workaround Example**

```
;*************************************************************************************************
; Isochronous Transfer Endpoint 1 Initialization Code
; > Use a direct address RAM location (eg. 30h) to store a value for setting or not setting RXFFRC bit:
; > [30h] = 0Ch ->not to set RXFFRC bit,
; > [30h] = 1Ch ->to set RXFFRC bit,
;*************************************************************************************************
ISO_EP1_INIT:                                   ; example endpoint 1 initialization routine
    mov                                         ; do not set RXFFRC bit when entering SOF ISR for the ;first time
    30h, #0Ch

    ;other Endpoint 1 initialization code
    ret
;*************************************************************************************************
; START OF FRAME (SOF) Interrupt Service Routine
;  > RXFFRC bit is set to release the isochronous data packet that was read in previous frame
;*************************************************************************************************
;
SOF_ISR:                                        ; example endpoint 1 isochronous transfer ISR
  push  EPINDEX
    mov   EPINDEX, #01h                         ; select iso endpoint 1
    mov   RXCON, 30h                            ; set or do not set RXFFRC bit depends on value ;in 30
    ; do not add additional instructions before this line; RXFFRC bit must be set before OUT token arrives
  push   PSW
  push   PSW1
  push   ACC
  push   R3
    clr    ASOF                 ;clear SOF interrupt flag
;
EP1_RX_ISOC:                                    ;example ISO receive processing routine
   jb     RXFIF0, EP1_RX_DATA_AVAIL
  jb     RXFIF1, EP1_RX_DATA_AVAIL
  mov    30h, #0Ch                              ; no iso data packet received, don't
                                                ;setRXFFRC bit in next frame
  ljmp   EXIT_SOF_ISR

(Continued)
```

**Figure 1. Isochronous Transfer RXCNTx Errata Firmware Workaround Example (Continued)**

```
;*****************************************************************************************************
; Start of Frame Interrupt Service Routine, Continued
;*****************************************************************************************************
;
EP1_RX_DATA_AVAIL:
  mov     30h, #1Ch                                   ; to set RXFFRC bit in next frame as it is read in ;this frame

  jnb     RXERR, EP1_NO_RX_ERROR                      ; jump to iso receive error handling routine
  ljmp    HANDLER_RX1_ERROR_X
;
EP1_NO_RX_ERROR:
  mov     A,  RXCNTL                                  ; get the receive count
      jz    EXIT_SOF_ISR
  mov     R3, A                                       ; temp storage of RXCNTL
;
RX_Loop_x:
  mov     A,   RXDAT                                  ; read the iso data received
 ; process the data here, such as save to memory etc
  djnz    R3, RX_LOOP_X
;
EXIT_SOF_ISR:                                         ; restore any registers used
 pop  R3
     pop    ACC
  pop    PSW1
  pop    PSW
  pop    EPINDEX
 reti
```

## 5. 8x931Ax, 8x931Hx Cold-Boot Errata

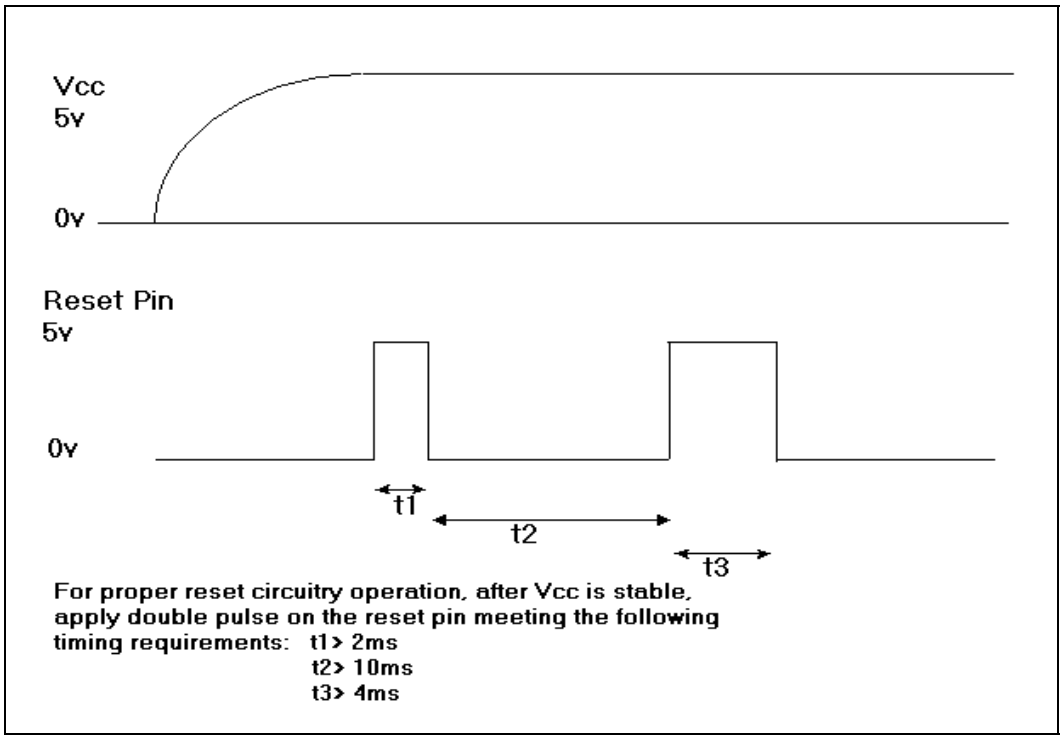
**Problem:** It has been discovered that members of the 8x931 USB Peripheral Controller family may not function after a cold-boot on certain PC systems. Intel has discovered on some PCs, that a small voltage (80mV – 1.0V) is present on the USB +5v connector pin when the system is powered off. This voltage coupled with 8x931 reset sensitivity can cause the 8x931 to fail to enumerate properly after a cold-boot power-on. This issue occurs when the "PC-off" USB supply voltage at the pin is between the range of 80mV – 200mV.

**Implication:** 8x931-based USB peripherals, when attached to a PC that has been cold-booted, may not enumerate after power-on if the PC provides partial power to the USB bus when powered off.

**Workaround 1:** The first method requires the end-user to unplug the affected peripheral from the PC and re-plug it back into the PC after a cold-boot power-on. This has proven to work properly on all systems tested to date.

**Workaround 2:** The second method entails the addition of reset circuitry which provides a double reset pulse instead of a single reset pulse at power-on. The reset signal shown in Figure 2 below has been characterized as a possible workaround for the cold-boot errata. Note that this reset pulse can be implemented in various manners. Intel is currently testing several of these methods and will publish them as part of this specification update when testing is completed. Note that use of this or any workaround should be validated by the implementer for given applications.

**Figure 2. Circuitry for Cold-Boot Errata**




**Status:** Fixed. Refer to “Summary Table of Changes” to determine the affected stepping(s).

# Specification Changes

## 1. The initial 8x931AA and 8x931HA devices will only be available in 68-pin PLCC packages

The 64-pin SDIP and 64-pin QFP packages mentioned in the 8x931AA/HA USB Peripheral Controller datasheet, product brief, and user's manual are currently unavailable. The production of these packages are still under evaluation.

## 2. ECAP usage to supply 3.0-3.1 volts for 1.5K pullup

Section 7.7 of the 8x931AA, 8x931HA datasheet incorrectly describes the ECAP voltage. This description was based on past steppings of the 8x930 controllers. For the 8x931, the ECAP pin and associated circuitry have been redesigned so that the ECAP voltage will be maintained at 3.0v to 3.1v instead of varying with VCC.

## 3. Reduced Float Waveform $I_{OL}/I_{OH}$ Load Value to +/-1mA

Figure 12 “Float Waveforms” on page 24 of the 8x931AA, 8x931HA Datasheet was changed to reflect a reduction to the $I_{OL}/I_{OH}$ load value. The higher current load (+/- 20mA) will cause the device to fail the float timings specs. Reduce the load to +/- 1mA.

## 4. Series Resistor Requirement for Impedance Matching Changed to 22 Ohms (no longer 27 – 33 ohms)

Section 7.3 of the 8x931AA, 8x931HA Datasheet has been changed. To better match the output driver impedance, the recommended resistance is 22 ohms.

# Specification Clarifications

## 1. P3.6 and P3.7 Low Going Spike

**Problem:** A 500mV low going spike can occur on P3.6 and P3.7, therefore causing these pins to NOT meet the following datasheet DC specification: VOH=Vcc - 0.3. This spike will happen only when a signal transition occurs on a Port 1 pin.

**Issue:** There is no application issue, even with this glitch, because these pins will not violate the VIH minimum specification for CMOS (3.5v) and TTL (2.0v) inputs.

**Affected Docs:** *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual* (order #: 273102), and *8x931AA/8x931HA Universal Serial Bus Peripheral Controller Datasheet* (order#: 273108).

## 2. PCON GF0 and GF1 Flags are Not Cleared on USB Reset

**Problem:** When not using USB reset separation, a USB reset should clear the GF0 and GF1 flags in the PCON register; this does not happen on 8x931xx devices.

**Issue:** Firmware designed to use these flags to determine when a USR reset occurs will not function properly. The GF0 and GF2 flags are only cleared on a full chip reset. This condition affects all steppings of the 8x931 devices.

**Workaround:** The programmer will need to utilize a different register or variable other than GF0 or GF1 if they are expecting them to be cleared on a USB reset.

**Affected Docs:** *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual* (order #: 273102), and *8x931AA/8x931HA Universal Serial Bus Peripheral Controller Datasheet* (order#: 273108).

# Documentation Changes

## 1. Change Name of Supply Voltage Pins from "$V_{CCP}$" to "$V_{CC}$".

**Issue:** The supply voltage pins are referred to as both $V_{CCP}$ and the $V_{CC}$. All references to $V_{CCP}$ pins in the text, tables, and pin maps are changed to $V_{CC}$.

**Affected Docs:** Appendices B and E of the *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual.*

## 2. Change Name of Circuit Ground Pins from "$V_{SSP}$" to "$V_{SS}$".

**Issue:** The circuit ground pins are referred to as both $V_{SSP}$ and $V_{SS}$. All references to $V_{SSP}$ pins in the text, tables, and pin maps are changed to $V_{SS}$.

**Affected Docs:** Appendices B and E of the *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual.*

## 3. Product Nomenclature

**Issue:** The "Device Speed" parameter in Figure 1 and Table 3 of the 8*x*931AA, 8*x*931HA Datasheet is incorrect. This parameter in the product name is used to identify the stepping revision for the device. For example, an 8x931HA0 is the A-0 stepping for the 8x931HA device, whereas 8x931HA1 would be the B-0 stepping for the same device.

**Affected Docs:** Figure 1 and Table 3 of the *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller Datasheet*.

## 4. QFP Package Information Added

**Issue:** Figures B-3 and B-4 and Tables B3 and B6 from the *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual* have been added below (see Figures 3 and 4 and Tables 1 and 2).

**Figure 3. 8x931HA 64-pin QFP Package**

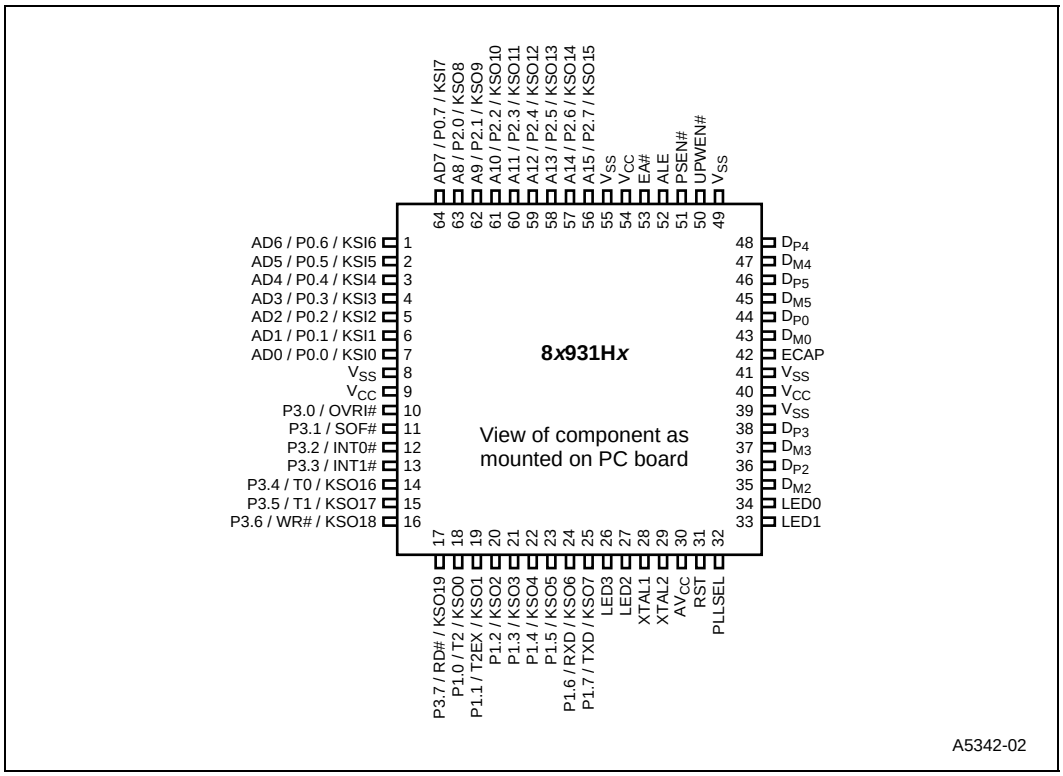
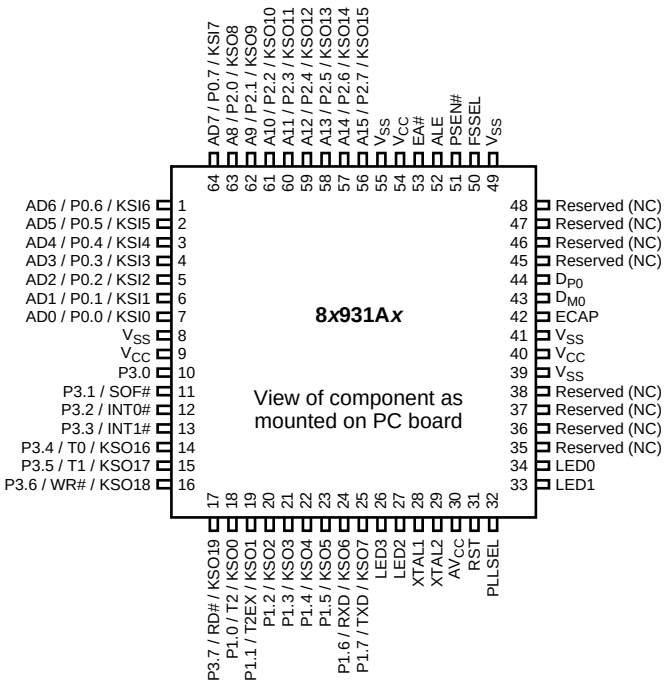


**Figure 4. 8x931AA 64-pin QFP Package**




**Notes:**
Reserved pins must be left unconnected..

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**Table 1. 64-pin QFP Pin Assignment**

| Pin | Name |
|---|---|
| 1 | AD6/P0.6/KSI6 |
| 2 | AD5/P0.5/KSI5 |
| 3 | AD4/P0.4/KSI4 |
| 4 | AD3/P0.3/KSI3 |
| 5 | AD2/P0.2/KSI2 |
| 6 | AD1/P0.1/KSI1 |
| 7 | AD0/P0.0/KSI0 |
| 8 | $V_{SS}$ |
| 9 | $V_{CC}$ |
| 10 | P3.0/OVRI#†† |
| 11 | P3.1/SOF# |
| 12 | P3.2/INT0# |
| 13 | P3.3/INT1# |
| 14 | P3.4/T0/KSO16 |
| 15 | P3.5/T1/KSO17 |
| 16 | P3.6/WR#/KSO18 |
| 17 | P3.7/RD#/KSO19 |
| 18 | P1.0/T2/KSO0 |
| 19 | P1.1/T2EX/KSO1 |
| 20 | P1.2/KSO2 |
| 21 | P1.3/KSO3 |
| 22 | P1.4/KSO4 |

| Pin | Name |
|---|---|
| 23 | P1.5/KSO5 |
| 24 | P1.6/RXD/KSO6 |
| 25 | P1.7/TXD/KSO7 |
| 26 | LED3 |
| 27 | LED2 |
| 28 | XTAL1 |
| 29 | XTAL2 |
| 30 | $AV_{CC}$ |
| 31 | RST |
| 32 | PLLSEL |
| 33 | LED1 |
| 34 | LED0 |
| 35 | Reserved (NC)†/$D_{M2}$†† |
| 36 | Reserved (NC)†/$D_{P2}$†† |
| 37 | Reserved (NC)†/$D_{M3}$†† |
| 38 | Reserved (NC)†/$D_{P3}$†† |
| 39 | $V_{SS}$ |
| 40 | Vcc |
| 41 | Vss |
| 42 | ECAP |
| 43 | $D_{M0}$ |
| 44 | $D_{P0}$ |

| Pin | Name |
|---|---|
| 45 | Reserved (NC)†/$D_{M5}$†† |
| 46 | Reserved (NC)†/$D_{P5}$†† |
| 47 | Reserved (NC)†/$D_{M4}$†† |
| 48 | Reserved (NC)†/$D_{P4}$†† |
| 49 | Vss |
| 50 | FSSEL†/UPWEN#†† |
| 51 | PSEN# |
| 52 | ALE |
| 53 | EA# |
| 54 | Vcc |
| 55 | $V_{SS}$ |
| 56 | A15/P2.7/KSO15 |
| 57 | A14/P2.6/KSO14 |
| 58 | A13/P2.5/KSO13 |
| 59 | A12/P2.4/KSO12 |
| 60 | A11/P2.3/KSO11 |
| 61 | A10/P2.2/KSO10 |
| 62 | A9/P2.1/KSO9 |
| 63 | A8/P2.0/KSO8 |
| 64 | AD7/P0.7/KSI7 |

† Specific to the 8x931AA

†† Specific to the 8x931HA

**Table 2. 64-pin QFP Signal Assignments Arranged by Functional Category**

| Address & Data | |
|---|---|
| **Name** | **Pin** |
| AD6/P0.6/KSI6 | 1 |
| AD5/P0.5/KSI5 | 2 |
| AD4/P0.4/KSI4 | 3 |
| AD3/P0.3/KSI3 | 4 |
| AD2/P0.2/KSI2 | 5 |
| AD1/P0.1/KSI1 | 6 |
| AD0/P0.0/KSI0 | 7 |
| A15/P2.7/KSO15 | 56 |
| A14/P2.6/KSO14 | 57 |
| A13/P2.5/KSO13 | 58 |
| A12/P2.4/KSO12 | 59 |
| A11/P2.3/KSO11 | 60 |
| A10/P2.2/KSO10 | 61 |
| A9/P2.1/KSO9 | 62 |
| A8/P2.0/KSO8 | 63 |
| AD7/P0.7/KSI7 | 64 |

| Input/Output | |
|---|---|
| **Name** | **Pin** |
| P3.0/OVRI#†† | 10 |
| P3.1/SOF# | 11 |
| P3.2/INT0# | 12 |
| P3.3/INT1# | 13 |
| P3.4/T0/KSO16 | 14 |
| P3.5/T1/KSO17 | 15 |
| P3.6/WR#/KSO18 | 16 |
| P3.7/RD#/KSO19 | 17 |
| P1.0/T2/KSO0 | 18 |
| P1.1/T2EX/KSO1 | 19 |
| P1.2/KSO2 | 20 |
| P1.3/KSO3 | 21 |
| P1.4/KSO4 | 22 |
| P1.5/KSO5 | 23 |
| P1.6/RXD/KSO6 | 24 |
| P1.7/TXD/KSO7 | 25 |

| USB | |
|---|---|
| **Name** | **Pin** |
| PLLSEL | 32 |
| ECAP | 42 |
| $D_{M0}$ | 43 |
| $D_{P0}$ | 44 |
| FSSEL†/UPWEN#†† | 50 |
| OVRI#†† | 10 |
| $D_{P2}$†† | 36 |
| $D_{M2}$†† | 35 |
| $D_{P3}$†† | 38 |
| $D_{M3}$†† | 37 |
| $D_{P4}$†† | 48 |
| $D_{M4}$†† | 47 |
| $D_{P5}$†† | 46 |
| $D_{M5}$†† | 45 |

| Processor Control | |
|---|---|
| **Name** | **Pin** |
| XTAL1 | 28 |
| XTAL2 | 29 |
| RST | 31 |
| P3.2/INT0# | 12 |
| P3.3/INT1# | 13 |

| Power & Ground | |
|---|---|
| **Name** | **Pin** |
| $V_{CC}$ | 9 |
| $AV_{CC}$ | 30 |
| $V_{SS}$ | 39,55 |
| Vcc | 40,54 |
| Vss | 8, 41,49 |

| Bus Control & Status | |
|---|---|
| **Name** | **Pin** |
| PSEN# | 51 |
| ALE | 52 |
| EA# | 53 |
| WR# | 16 |
| RD# | 17 |

† Specific to the 8x931AA

†† Specific to the 8x931HA

## 5. Reset Circuitry Referred to in the Cold Boot Errata Added

**Issue:** The cold boot errata external circuit workaround diagram (83931HA1/83931AA1 Cold Boot Errata) has been added below (see Figure 1). Refer to "8x931Ax, 8x931Hx Cold-Boot Errata" on page 13 for more information.

The following resetsignal conditioning circuit is recommended to work around the power on cold boot erratаon 83931HA1/83931AA1 devices. This circuit consists of two stages. The first stage is the Vcc detect circuit that outputs a logic high value on vdet_out when Vcc rises to approximately 3.0 volts. The second stage is the double reset pulse generation circuit that creates two separate reset pulses on the reset output. The three time constants t1, t2 and t3 were chosen to meet the device reset requirements and still allow normal device operation within 10ms of Vcc rise (as per USB specification). The circuit has been tested and shown operational with Vcc ramp times from 1us (hot-plug) to 35ms (worse case PC power-on). Note that it is the responsibility of the implementor to validate the functionality/applicability of this workaround in their applications.

**Affected Docs:** *8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual* (order #: 273102), and *8x931AA/8x931HA Universal Serial Bus Peripheral Controller Datasheet* (order#: 273108).

**Figure 1. 83931HA1/83931AA1 Cold Boot Errata External Reset Circuit Workaround**